



SHA256

SHA-256 Secure Hash Function Megafunction

The SHA256 megafunction is a high-performance implementation of the SHA-256 Secure Hash message digest Algorithm. This one-way hash function conforms to the 1995 US Federal Information Processing Standard (FIPS) 180-2. It accepts a large, variable-length message and produces a fixed-length message authorization code.

The megafunction is composed of two main modules, the SHA256 Engine Module and the Input Interface Module as shown in the block diagram. The SHA256 Engine Module applies the SHA256 loops on a single 512-bit message block, while the Input Interface Module performs the message padding.

The processing of one 512-bit block is performed in 66 clock cycles and the bit-rate achieved is 7.75Mbps / MHz on the input of the SHA256 megafunction.

The SHA256 megafunction is equipped with fully-stallable input and output interfaces. These enable the user's application to stop the input stream according to a data arrival rate, or to stop the output stream when the megafunction is not able to receive data.

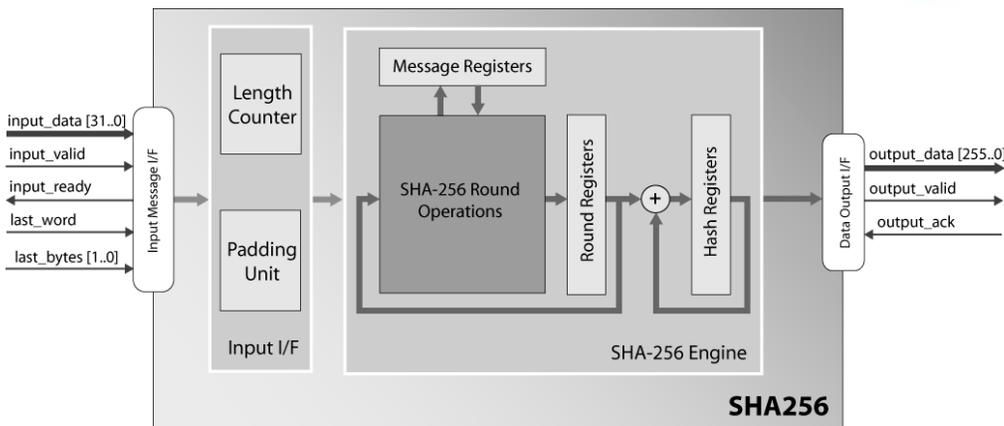
The megafunction has been evaluated in a variety of technologies, and is available optimized for ASICs or FPGAs. Representative results show that the megafunction fits in a variety of Altera devices, requiring, for example, about 2,531 LEs for Cyclone. The complete deliverables feature comprehensive documentation, and a bit-accurate software model (BAM).

Applications

The megafunction is suitable for a variety of applications requiring digital signatures or other message origin authentication or tamper protection, including:

- E-commerce
- Data integrity
- Bulk Encryption
- High speed networking equipment
- Secure wireless applications

Block Diagram



Features

- Compliant to FIPS 180-2 specification of SHA-256.
- Bit padding.
- $2^{64}-1$ bits maximum message length.
- Supported Message lengths multiple of 8-bits.
- Initial values of Chaining Variables selected before synthesis.
- 66 processing cycles per message block.
- Fully stallable input and output interfaces, ideal for streaming applications.
- Optimized design for ASIC or FPGA implementations.
- Robust verification environment includes bit-accurate software model.
- Scan-ready design architecture

Functional Description

The input message data is passed in 32-bit words to the megafunction, masked with the input_valid signal. As long as the input_ready signal is active, the external application should keep feeding input data to the megafunction. When the megafunction has received a complete message 512-bit packet, it pauses the input stream, and continues the message processing internally. When the message is processed and the megafunction is ready for the next message, the megafunction permits input data to be fed again. On the final message block, when the last 32-bit word is written, the last_word input must be activated, to indicate that a hash value has to be generated to the megafunction's output. Along with the last_word, the last_bytes input must indicate how many bytes are valid in the last word, so that the padding unit knows how many bytes to pad.

The megafunction can easily be modified to support programmable Initial Vectors for the Chaining Variables in place of the constants defined in the algorithm's specification.

Implementation Results

The following are sample Altera results with all I/Os assumed to be routed off-chip.

Family Device	Fmax (MHz)	Logic	Throughput (Mbps)	Quartus Version
Arria EP1AGX50-6	92	2,131 ALUTs 1 M4K	713	8.1
Cyclone 1C12F324-6	106	2,531 LEs	821	7.1
Cyclone-II 2C20F484-6	108	2,436 LEs	837	7.1
Cyclone-III 3C16F484-6	109	2,416 LEs	844	7.1
Stratix 1S10F484-5	109	2,513 LEs	844	7.1
Stratix-II 2S15F484C3	158	2,531 ALUTs	1224	7.1
Stratix-III 3SE50F484-2	176	2,505 ALUTs	1364	7.1
Hardcopy HC210F484C	152	16,643 Hcells	1178	7.1

Export Permits

This encryption technology is governed internationally by export regulations. Immediate export of the megafunction is permitted to the following countries for uses not related to weapons of mass destruction:

Argentina	Japan	South Korea
Australia	New Zealand	Switzerland
Canada	Norway	Turkey
European Union Member States	Russia	Ukraine
		United States

Please contact CAST to discuss delivery to other destinations; approval is subject to the applicable export licenses being granted. The license can be generated from either the EU or the USA. Please note that licensees are responsible for complying with the applicable requirements for re-export of electronics containing strong encryption technology.

Support

The SHA256 megafunction as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The SHA256 megafunction has been verified through extensive simulation and rigorous code coverage measurements. It has also been verified in a prototyping FPGA board platform.

Deliverables

The SHA256 is available as a soft megafunction (synthesizable HDL) for ASIC technologies and as a firm megafunction (netlist) for FPGA technologies, and includes everything required for successful implementation. The Altera version includes:

- Post Synthesis EDIF.
- Place and route scripts.
- Simulation script, vectors and expected results.
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001).
- Software (C++) Bit-Accurate Model.
- Comprehensive user documentation, including detailed specifications and a system integration guide.

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The SHA256 megafunction is sourced from
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